IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

Rejections of Claims 2 and 20 Under 35 U.S.C. §112, Second Paragraph.

Applicant respectfully requests that this ground for rejection be reconsidered.

The rejection has found the term "linearly aligned" to be indefinite.

While this term is believed to be understood by its ordinary and customary meaning, Applicant notes that very particular examples of such arrangements are explicitly described in a numerous locations within Applicant's Specification:

> Also, as shown in FIG. 3, "n" input delay circuits **111** and "n/2" output delay circuits **112**, including a DLL, and the like, can be arranged between the *linear aligned* data/signal I/O terminals (**105/106**) and *linear aligned* first stage and final stage FFs (**107/108**). (Applicant's Specification, Page 15, Lines 19-22, emphasis added).

> Accordingly, in the case where such output delay circuits **112**, signal I/O terminals **106**, final stage FFs **108**, and output delay circuits **112** (and/or input delay circuits **111**) are *linear aligned* as set forth in FIG. 7, the output of delay circuits **112** can be made in close proximity with signal I/O terminals **106**. (Applicant's Specification, Page 24, Lines 18-21, emphasis added).

Accordingly, reference to FIGS. 3 and 7 of Applicant's Specification would show one very particular example of "linear aligned".

Importantly, the above examples should not necessarily be construed as limiting to Applicant's invention. The examples represent but particular embodiments of the invention.

Rejection of Claims 1, 5, 7-19 and 21 Under 35 U.S.C. §102(e) based on *Yanagawa* (US Patent Application Publication 2001/0046163 A1).

The rejection of claims 1, 5, and 7-14 will first be addressed.

The memory controller of claim 1 includes a clock generating circuit, a data generating circuit, a predetermined number "m" data output terminals, m output holding circuits, a predetermined number "n" signal output terminals, and a plurality of output delay circuits. The

clock generating circuit generates an output clock signal. The data generating circuit provides output digital data. The predetermined number "m" data output terminals provide output data to the semiconductor memory device in parallel. The m output holding circuits store the output digital data synchronously with the output clock signal. The predetermined number "n" signal output terminals provide output strobe signals to the semiconductor memory device in synchronism with the output data, where $n < m$. The plurality of output delay circuits include one output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s). Each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals. The output of each output delay circuit is adjacent to the corresponding p signal output terminal(s).

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the reference *Yanagawa* does not show all elements of claim 1, this ground of rejection is traversed.

Yanagawa discloses a memory controller that provides an interface between a microprocessor having a 64-bit data width and a memory device that has a 32-bit data width. The controller includes latch circuits (30 and 31), alleged to correspond to Applicant's m output holding circuits[1] that each latch a 32-bit half of the 64-bit data supplied from the microprocessor.[2]

However, Applicant does not believe that the latch circuits of *Yanagawa* are ever shown or suggested to be "physically adjacent to a corresponding one of the m data output terminals", as recited in claim 1. To show these claim 1 limitations, the rejection relies on the following reasoning:

> Wherein each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals [figures 2, 5-7] (Office Action, dated 10/12/2005, Page 4, Lines 3-6)[3]

However, Applicant notes that while Figure 2 of *Yanagawa* shows a block diagram of the

[1] See Page 3, lines 11-12 of Office Action dated October 12, 2005.
[2] See FIG. 2 in conjunction with paragraph [52] of *Yanagawa*.
[3] See Page 4, lines 3-6 of Office Action dated October 12, 2005.

controller 10, there is no place in the written description indicating a physical location of such latch circuit (30 and 31) with reference to any output terminals. In fact, no output terminals are shown in this figure. Figure 2 of *Yanagawa* only shows a 32 bit bus (DATA(32bit)) for data between memory device 11 and controller 10 without any indication as to presence of, let alone physical location of, and data output terminals.

While the rejection cites Figures 5-7, these figures do not show or suggest a physical location of either latch circuits or data output terminals. Figures 5-7 are circuit diagrams showing various aspects of delay control circuit, phase comparator circuit, and variable delay circuits of Figure 3. These figures do not provide teachings related to latch circuits (30 and 31) and/or data output terminals.

Accordingly, because *Yanagawa* does not show all elements of claim 1, this ground of rejection is traversed.

Claim 8, which depends indirectly from claim 1, recites "first and second wiring corresponding to each input holding circuit being essentially equal in length". In a similar fashion, Claim 14, which depends indirectly from claim 1, recites "the length of the first wiring to each second latch circuit is essentially equal to the sum of the lengths of the second and third wirings".

The rejection reasoning for these claims cites paragraphs [0060] to [0064] of *Yanagawa* to show such limitations.[4] However, Applicant's review of these paragraphs shows no mention of wiring lengths. Accordingly, the rejection cannot have established a prima facie case for this claim.

The rejection of claims 15-19 will now be addressed.

The memory controller of claim 15 includes a predetermined number "m" data input terminals, a predetermined "n" signal input terminals, a data storing circuit, n input delay circuits, m input holding circuits, m signal input wirings and m signal input wirings. The predetermined number "m" data input terminals receive input data from the semiconductor memory device. Each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data, where $m > n$. The data storing circuit receives digital data from the data input terminals. The n input delay circuits delay received device input clock signals from the semiconductor memory device by a predetermined

[4] See the Office Action, dated 10/12/2005, Page 6, Lines 16-17.

amount to generate input strobe signals. The m input holding circuits hold the input data in synchronism with the input strobe signals generated by the input delay circuits. Each data input wiring transmits an input data value from one data input terminal to a corresponding input holding circuit. The m signal input wirings transmit one input strobe signal from one input delay circuit to a corresponding input holding circuit. The data input wiring and signal input wiring for the same corresponding input holding circuit being essentially equal in length.

The cited reference *Yanagawa* discloses a memory controller that provides an interface between a microprocessor having a 64-bit data width and a memory device that has a 32-bit data width. The controller includes latch circuits (27), argued to correspond to Applicant's m input holding circuits[5] that latch a 32-bit data supplied from the memory device.[6]

However, Applicant does not believe that *Yanagawa* does not show a data input wiring and signal input wiring for the same corresponding holding circuit being "essentially equal in length" as recited in claim 15.

To address this ground for rejection, Applicant incorporates by reference herein the comments set forth above for claims 8 and 14 are incorporated by reference herein.

Accordingly, because *Yanagawa* does not show all elements of claim 15, this ground of rejection is traversed.

Rejection of Claims 3, 4, and 6 Under 35 U.S.C. §103(a), based on *Yanagawa* in view of *Kuge* (US Patent Application Publication 2001/0014922 A1).

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[7]

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[8]

To the extent that this ground for rejection relies on *Yanagawa*, the arguments set forth above with respect to claim 1 are incorporated herein by reference. Namely, *Yanagawa* does not show each m output holding circuit is physically adjacent to a corresponding one of the m data

[5] See Page 3, lines 11-12 of Office Action dated October 12, 2005.
[6] See FIG. 2 in conjunction with paragraph [53] of *Yanagawa*.
[7] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).
[8] MPEP §2143.

output terminals. Though not relied upon by the rejection to show such limitations, *Kuge* also does not teach such a limitation element.

For this reason this ground for rejection is traversed.

The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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